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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/564,473	01/13/2006	Masaki Murase	SON-3058	9263

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EXAMINER	
SITTA, GRANT	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/564,473	MURASE ET AL.	
	Examiner	Art Unit	
	GRANT D. SITTA	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/10/2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 June 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 7-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of JP Iemoto Hiroshi (2000-191367) hereinafter, Iemoto.

4. In regards to claim 7, AAPA teaches a display device comprising:

a level shifter (fig. 1 (1)) configured to change an amplitude of gradation data from a first voltage range to a second voltage range (fig. 2 (b) and (c)), amplified gradation data being said gradation data at said second voltage range [0009-0010],

output data during a period other than said quiescent period being said amplified gradation data (fig. 2 (c)).

AAPA fails to teach wherein output data during a quiescent period is dummy data.

However, Iemoto teaches wherein output data during a quiescent period is dummy data (Abstract, (0008—0012, 0082-0084]).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to incorporate the dummy data during a quiescent period as taught by Iemoto in order to reduce fluctuations in the operating frequency of the circuit as stated in the abstract of Iemoto

5. In regards to claim 8, AAPA teaches the display device according to claim 7, wherein a maximum value of said first voltage range is lower than a maximum value of said second voltage range (fig. 2 A-C).

6. In regard to claim 9, AAPA teaches the display device according to claim 7, wherein said first voltage range is 0 volts to 3 volts and said second voltage range is 0 volts to 6 volts (fig. 2 B-C).

7. In regards to claim 10, AAPA teaches the display device according to claim 7, wherein said quiescent period is during which said gradation data is held at a constant logical level for a constant period at a constant cycle (fig. 2 (B-C) T2).

8. In regards to claim 11, AAPA as modified by Iemoto teaches the display device according to claim 10, wherein said dummy data has a logical level opposite to said constant logical level (Abstract, (0008—0012, 0082-0084] Iemoto) .

9. AAPA does not disclose expressly wherein said quiescent period is a horizontal blanking period.

However, Applicant has not disclosed that having wherein said quiescent period is a horizontal blanking period instead of a vertical blanking period [0010] provides an advantage, is used for a particular purpose, or solves a stated problem. As such, having quiescent period is a horizontal blanking period is an obvious matter of design choice.

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have quiescent period is a horizontal blanking period because either configuration would perform equally well at providing the predictable result of providing dummy data during a blanking period to avoid various influences due to the variation in delay time and provide for a desirable display.

10. In regards to claim 13, AAPA teaches the display device according to claim 10, wherein said quiescent period is a vertical blanking period ([0010] AAPA).

11. In regards to claim 14, AAPA teaches the display device according to claim 10, wherein said gradation data is video data [0002-0010].

12. In regards to claim 15, AAPA teaches the display device according to claim 7, wherein said amplitude of the output data is changed from said second voltage range to said first voltage range, resultant gradation data being said output data at said first voltage range [0007-0011] (fig. 2 B-C).

13. In regards to claim 16, AAPA teaches the display device according to claim 15, wherein said resultant gradation includes said output data that has been latched on a rising edge of a sampling pulse [0007-0011] (fig. 2 td1 and fig. 3).

14. In regards to claim 17, AAPA teaches the display device according to claim 16, wherein said resultant gradation includes said output data that has been latched on a falling edge of a sampling pulse (fig. 3 (a) and falling edge).

15. In regards to claim 18, AAPA teaches the display device according to claim 15, wherein a horizontal driving circuit converts said resultant gradation data into analog signals [0006].

16. In regards to claim 19, AAPA teaches the display device according to claim 18, wherein a vertical driving circuit sequentially selects pixels through gate lines, said

pixels selected through said gate lines being driven by said analog signals [0006].

17. In regards to claim 20, AAPA teaches the display device according to claim 19, wherein said pixels are arranged in a matrix form [0005].

18. In regards to claim 21, AAPA teaches the display device according to claim 7, wherein an active device for processing said resultant gradation data is formed by low-temperature polysilicon [0008].

19. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Iemoto, in view of Ochiai et. al (US 6,897,909) hereinafter, Ochiai.

20. In regards to claim 5, AAPA and Iemoto differ from the claimed invention in that AAPA and Iemoto do not disclose wherein an active device for processing said resultant gradation data is formed by continuous grain silicon.

However, Ochiai teaches a system and method wherein an active device for processing said resultant gradation data is formed by continuous grain silicon (col. 23, lines 39-52).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify AAPA and Iemoto to include the use of an active devices for processing the gradation data is formed by CGS as taught by Ochiai in order to

implement smaller sized TFTs which save space and enable more light to pass through to the view for better picture quality.

Response to Arguments

21. Applicant's arguments with respect to claim7-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

22. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GRANT D. SITTA whose telephone number is (571)270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Grant D Sitta/
Examiner, Art Unit 2629
August 12, 2009

/Richard Hjerpe/
Supervisory Patent Examiner, Art Unit 2629